PATENT C'afC 2814

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

ent Number:

6,727,143 B1

Issued:

April 27, 2004

Name of Patentee:

Hui et al.

Assignee:

Advanced Micro Devices, Inc., Fujitsu Limited,

Fujitsu and Semiconductor Ltd.

Title of the Invention: METHOD AND SYSTEM FOR

REDUCING CHARGE GAIN AND CHARGE LOSS WHEN USING AN ARC LAYER IN INTERLAYER DIELECTRIC FORMATION

#### **CERTIFICATION UNDER** 37 C.F.R. § 1.8

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Serena Beller

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Kelly K. Kordzik Winstead Sechrest & Minick P.C. P.O. Box 50784

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Since the Certificate of Correction is necessary to correct mistakes made by the 3. PTO in printing this patent, Patentees are not required to submit a fee herewith.

Respectfully submitted,

WINSTEAD SECHREST & MINICK P.C.

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# UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO. : 6,727,143 B1 DATED : April 27, 2004

INVENTOR(S): Angela T. Hui; Mark T. Ramsbey; Yu Sun; David H. Matsumoto

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 1, Line 28, following "which" please delete "is".

Column 1, Line 51, following "ARC" please delete "so".

Column 3, Line 4, following "further" please delete "so".

Column 6, Line 29, following "to the" please delete "in".

MAILING ADDRESS OF SENDER: Winstead Sechrest & Minick P.O. Box 50784 Dallas, Texas 75201 PATENT NO. \_\_\_\_6,727,143 B1\_\_\_\_ No. of add'l copies @ 50¢ per page

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